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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 57941.000063	SERIAL NUMBER 10/716,596
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
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	118.	5,023,488	06/11/91	Gunning			
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	122.	4,821,226	04/11/89	Christopher et al.			
	123.	4,882,712	11/21/89	Ohno et. al.			
	124.	4,951,251	08/21/90	Yamaguchi et al.			
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	128.	M. Bazes, A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983)
	129.	D. Wendell et al., "A 3.5ns Self Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50
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	131.	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989)
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